

OEM 107 (2ST/EPW26)

Lecteur 13.56 MHz

Guide d'installation

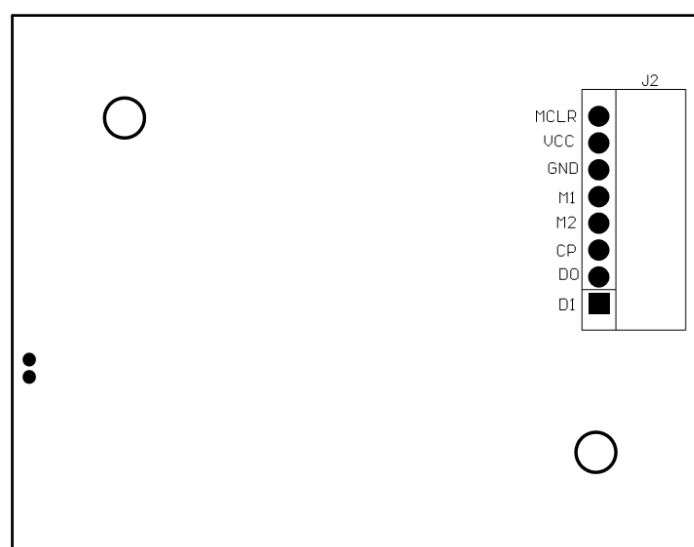
Version 1



1 Spécifications

Cartes compatibles	Mifare UID
Encodage	Manchester 64-bit, modulus 64
Interface	Wiegand26, RS232-TTL, Clock&Data
Alimentation	5 VDC; 55mA Max
Antenne	Antenne intégrée
Dimensions	52 x 40.2 mm
Températures	de -20°C à +60°C
Reading range	>4cm, selon transpondeur

2 Connecteurs



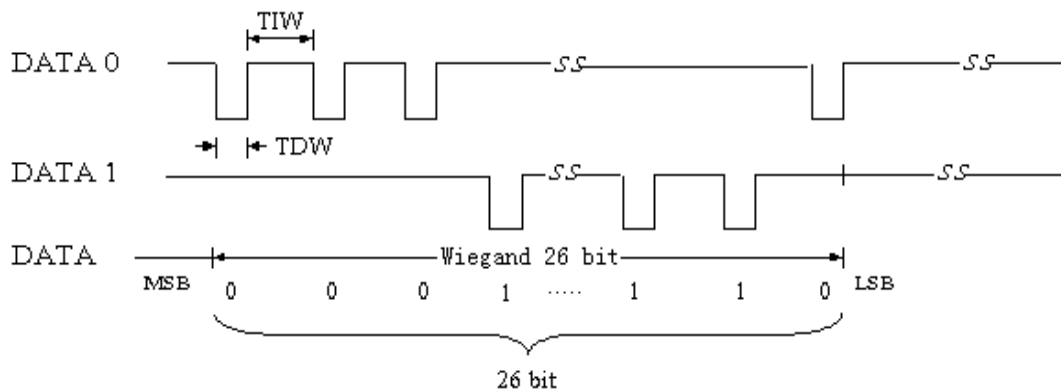
Description	RS232-TTL	Clock&Data10	Clock&Data8	Wiegand26
MCLR	---	---	---	---
VCC	5V	5V	5V	5V
GND	GND	GND	GND	GND
M1	---	---	Connecté GND	Connecté GND
M2	---	Connecté GND	---	Connecté GND
CP	---	CP	CP	CP
D0	TX	Clock	Clock	D0
D1	---	Data	Data	D1

3 Format Wiegand 26

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
Note	P	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	P
	P	E	E	E	E	E	E	E	E	E	E	E	E														
														O	O	O	O	O	O	O	O	O	O	O	O	O	P

Note:

E: Even 0: odd P: parity bit D: DATA



SYMBOL	Parameter	Limits Min.	Limits Max.	Type	UNITS
TDW	Data Pulse width time	20	100	50	µS
TIW	Data Pulse interval time	0.2	4	2	mS

4 RS232-TTL format (HEX)

- 1) Baud rate: 9600bps
- 2) Parity: no
- 3) Data bits: 8
- 4) Stop bits: 1

5 Clock And Data (Europe) Protocol

5.1 Description

The protocol provides a 3-wire Clock and Data (**Europe**) interface with a 10 digit BCD or 8 digit BCD Tag Code. The three wires are defined as Presence, Clock and Data. The Presence line will indicate the presence of a Tag. The Clock line is used to clock the data on the Data line.

5.2 Protocol

Clock&Data 10:

A 10-Digit BCD number transmits the 32 bit Code with a Start and Stop sentinel and Longitudinal Redundancy Check (LRC) checksum defined as follows:

BCD 0	BCD 1 to 10	BCD 11	BCD 12
Start	32 bit code as BCD	Stop	LRC Checksum
B (Hexadecimal)	NNNNNNNNNN	F (Hexadecimal)	X

Where N = 0 to 9

Each BCD Digit has an odd-parity bit appended:

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
LSB of BCD			MSB of BCD	Odd Parity
1	0	0	1	1

The LRC checksum is calculated by XOR the BCD Digits including the Start and Stop Sentinel but excluding the parity bits. The parity of the LRC checksum is also set to odd-parity, For example:

BCD	Binary	Parity
B	1011	0
5	0101	1
7	0111	0
0	0000	1
1	0001	0
9	1001	1
3	0011	1
5	0101	1
1	0001	0
F	1111	1
LRC	1001	1

Clock&Data 8:

The 24 bit Code is transmitted by a 8 Digit BCD number with a Start and Stop sentinel and Longitudinal Redundancy Check (LRC) checksum defined as follows:

BCD 0	BCD 1 to 8	BCD 9	BCD 10
Start	24 bit code as BCD	Stop	LRC Checksum
B (Hexadecimal)	NNNNNNNN	F (Hexadecimal)	X

Where N – 0 to 9

Each BCD Digit is appended with an odd-parity bit as defined above. The LRC checksum is calculated as above.

The 13-Digit or 11-Digit BCD number is transmitted serially on the Data signal line starting with BCD-0's LSB. If a bit is equal to a One the Data signal line is at GND. If the bit is equal to a Zero the Data signal line is at Vcc.

The timing of the Clock and Data (**Europe**) protocol is shown in Figure 2.

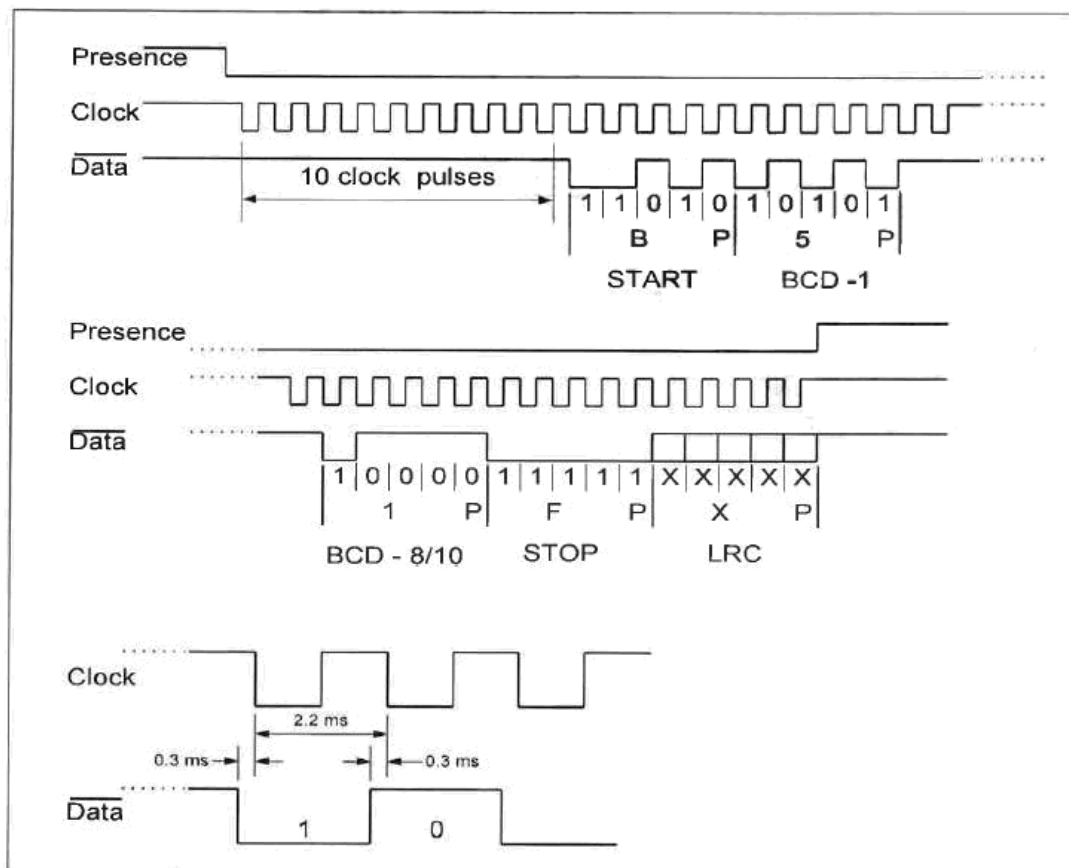


Figure 2